WHAT IS CLAIMED IS:

1. A processor comprising:

5   a queue configured to store one or more instructions; and

a control circuit coupled to the queue, wherein the control circuit is configured to
detect a replay of a first instruction due to a dependency on a load miss,
and wherein the control circuit is configured to inhibit issuance of the one

10   or more instructions in the queue to one or more pipelines of the processor
responsive to detecting the replay.

2. The processor as recited in claim 1 wherein the control circuit is configured to inhibit
issuance of the one or more instructions until fill data is provided to a data cache of the

15   processor.

3. The processor as recited in claim 2 wherein the fill data corresponds to the load miss.

4. The processor as recited in claim 3 wherein the control circuit includes a storage

20   device, and wherein the control circuit is configured to read a miss tag from a read queue
that stores one or more load misses, the miss tag identifying the load miss on which the
first instruction is dependent, and wherein the control circuit is configured to store the
miss tag in the storage device, and wherein the control circuit further includes a
comparator coupled to the storage device and coupled to receive a fill tag identifying fill

25   data being provided to the data cache, and wherein the comparator is configured to
compare the miss tag stored therein to the fill tag to determine if the fill data corresponds
to the load miss.

5. The processor as recited in claim 2 wherein the fill data corresponds to any load miss.

6. The processor as recited in claim 1 wherein the control circuit is configured to permit issuance of the one or more instructions in response to fill data being provided to a data cache of the processor.

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7. The processor as recited in claim 6 wherein the fill data corresponds to the load miss.

8. The processor as recited in claim 7 wherein the control circuit includes a storage device, and wherein the control circuit is configured to read a miss tag from a read queue

10   that stores one or more load misses, the miss tag identifying the load miss on which the first instruction is dependent, and wherein the control circuit is configured to store the miss tag in the storage device, and wherein the control circuit further includes a comparator coupled to the storage device and coupled to receive a fill tag identifying fill data being provided to the data cache, and wherein the comparator is configured to

15   compare the miss tag stored therein to the fill tag to determine if the fill data corresponds to the load miss.

9. The processor as recited in claim 6 wherein the fill data corresponds to any load miss.

20   10. The processor as recited in claim 6 wherein the control circuit is configured to permit issuance of one of the one or more instructions if one or more issue criteria are fulfilled for that instruction.

11. The processor as recited in claim 10 wherein the one or more issue criteria includes a

25   lack of dependencies being detected for that instruction in one or more scoreboards coupled to the control circuit.

12. The processor as recited in claim 1 wherein the control circuit is configured to detect the dependency of the first instruction on the load miss using one or more scoreboards

which track instructions that have passed a first stage of the one or more pipelines, wherein the first stage is the stage at which replay is signaled.

13. The processor as recited in claim 1 wherein the one or more instructions in the queue include the first instruction.

14. A method comprising:

detecting a replay of a first instruction due to a dependency on a load miss; and

inhibiting issuance of one or more instructions from a queue to one or more pipelines of the processor responsive to detecting the replay.

15. The method as recited in claim 14 further comprising inhibiting issuance of the one or more instructions until fill data is provided to a data cache.

16. The method as recited in claim 15 wherein the fill data corresponds to the load miss.

17. The method as recited in claim 16 further comprising:

reading a miss tag from a read queue that stores one or more load misses, wherein the miss tag identifies the load miss on which the first instruction is dependent; and

comparing the miss tag to a fill tag identifying the fill data to determine if the fill data corresponds to the load miss.

18. The method as recited in claim 15 wherein the fill data corresponds to any load miss.

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19. The method as recited in claim 14 further comprising permitting issuance of the one or more instructions in response to fill data being provided to a data cache of the processor.

5   20. The method as recited in claim 19 wherein the fill data corresponds to the load miss.

21. The method as recited in claim 20 further comprising:

reading a miss tag from a read queue that stores one or more load misses, wherein

10   the miss tag identifies the load miss on which the first instruction is dependent; and

comparing the miss tag to a fill tag identifying the fill data to determine if the fill data corresponds to the load miss.

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22. The method as recited in claim 19 wherein the fill data corresponds to any load miss.

23. The method as recited in claim 19 wherein the permitting issuance of one of the one or more instructions is responsive to one or more issue criteria being fulfilled for that

20   instruction.

24. The method as recited in claim 23 wherein the one or more issue criteria includes detecting a lack of dependencies for that instruction in one or more scoreboards.

25   25. The method as recited in claim 14 wherein the detecting the dependency comprises checking one or more scoreboards which track instructions that have passed a first stage of the one or more pipelines, wherein the first stage is the stage at which replay is signaled.

26. The method as recited in claim 14 wherein the one or more instructions in the queue include the first instruction.

27. A more carrier medium comprising one or more data structures representing a processor including:

a queue configured to store one or more instructions; and

a control circuit coupled to the queue, wherein the control circuit is configured to detect a replay of a first instruction due to a dependency on a load miss, and wherein the control circuit is configured to inhibit issuance of the one or more instructions in the queue to one or more pipelines of the processor responsive to detecting the replay.